REMARKS

Claims 1-20 remain pending in the present application. Claim 7 has been amended. Applicants respectfully request reconsideration of the application in view of the foregoing amendment and the remarks appearing below.

Objection to Drawings under 37 C.F.R. § 1.83(a)

The drawings stand objected to under 37 C.F.R. § 1.83(a) as failing to "show every feature of the invention specified in the claims." In particular, the Examiner objects to the drawings as failing to show a "pulse generator." Applicants respectfully disagree.

Applicants respectfully assert that the drawings indeed show a pulse generator. For example, in FIG. 4 the operation of AND gate 224 in conjunction with inverter 220 generates a pulse as a function of clock signal CLK2. Correspondingly, the written description of FIG. 4 at lines 28-29 on page 5 explicitly states that FIG. 4 shows a "circuit element 224, e.g., an AND gate, that generates a clock pulse 228 . . ." Even without these explicit words, Applicants respectfully submit that those of ordinary skill in the art will readily recognize the pulse generating character of AND gate 224 in the context of the shift register latch of the present application. FIGS. 5A-C similarly explicitly show pulse generators.

In view of the foregoing, Applicants respectfully request that the Examiner withdraw the present objection to the drawings.

Rejection Under 35 U.S.C. § 102(b)

Claims 1-2, 5-7, and 10-13 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,304,122 to Gregor et al., stating that Gregor et al. disclose all of the limitations of these claims. Applicants respectfully disagree.

Gregor et al. disclose a flip-flop device having fewer clock trees than prior devices and that supports Level Sensitive Scan Design (LSSD) functionality. In relevant part, Gregor et al. disclose a shift-register latch 1140 (FIGS. 11 and 15) that includes a master latch 1520 (FIG. 15) and a slave latch 1530. Located external to shift-register latch 1140 is a flushable single clock splitter 1130 (FIG. 11) that provides two clock signals L1 Clock, L2 Clock to master latch 1520 and slave latch 1530, respectively.

Claims 1, 2, 3, 5, and 6

Applicants respectfully submit that Gregor et al. do not disclose or suggest the subject matter of independent claim 1, nor claims 2, 5, and 6 that depend therefrom. For example, independent claim 1 requires in its body "at least one shift register latch, comprising . . . a first latch . . . an input for receiving a first clock signal; and . . . a circuit, connected between said input and said first latch configured for generating a second clock signal . . . ." This language explicitly requires that the shift register latch itself have an input and contain the first latch. It also requires that the shift register latch contain the second-clock-generating circuit between the input and the first latch.

Referring to Gregor et al. FIGS. 11 and 15, it is readily seen in stark contrast that the flushable single clock splitter 1130 that is asserted to be within the shift register latch is in fact an external component to the shift register latch. Since the Gregor et al. shift register latch in fact does not contain a second-clock-signal generating circuit, the Gregor et al. patent cannot anticipate independent claim 1, nor claims 2, 3, 5, and 6 that depend therefrom.

In addition, independent claim 1 requires that the circuit connected between the input and first latch of the shift-register latch be "configured for generating a second clock signal that compensates for any delay in the said first clock signal," which is received at the input to the shift register latch, as seen in claim 1. While the Gregor et al. flushable single clock splitter 1130 is provided to generate two clock signals from one clock signal where one of the two generated clock signals is delayed relative to the other, splitter 1130 cannot reasonably be considered to compensate for any delay in a first clock signal. See the Gregor et al. patent, col. 7, line 54 to col. 8, line 11.

Since the Gregor et al. patent does not include all of the limitations of independent claim 1, this claim and claims 2, 5, and 6 that depend therefrom cannot be anticipated by the Gregor et al. patent.

In addition, regarding claims 5 and 6, Applicants fail to see how FIG. 13 and the passage at col. 8, lines 6-20 support the Office Action's position that Gregor et al. teach that the pulses of a second clock signal are shorter in duration than the pulses of a first clock signal. FIG. 13 does not show this and the passage does not describe this. For this additional reason, the Gregor et al. patent cannot anticipate claims 5 and 6.

Furthermore, regarding claim 3, this claim requires the circuit (which, again, is located between the input to the shift-register latch and the first latch) to have a "pulse generator." The Office Action asserts that Gregor et al. disclose a pulse generator at the single clock in FIG. 11. First, Applicants assert that it is not reasonable in the art to say that the Gregor et al. single clock is part of the shift-register latch. Gregor et al. themselves designate the shift-register latch as element 1140, which is wholly separate and distinct from the single clock. Anyone of ordinary skill in the art would likewise make such a distinction.

Second, using the Office Action's rational for rejecting claim 1, (which is incorrect) the Gregor et al. circuit corresponding to the compensating circuit of claim 1 is the clock splitter 1130 (FIG. 11). This splitter 1130 creates the clock signal for the master latch 1520 (FIG. 15) from the single clock signal. Consequently, the single clock is not the clock signal L1 Clock for master latch 1520. Claim 3, in contrast, requires that the pulse generator is "for generating a first clock pulse for said first latch." [Emphasis added.] Any reasonable interpretation of the preceding underlined portion requires the pulse generator to be immediately upstream from the first latch, not at least once removed through clock splitter 1130. For this additional reason, the Gregor et al. patent cannot anticipate claim 3.

For at least the foregoing reasons, Applicants respectfully request that the Examiner withdraw the present rejection of claims 1, 2, 3, 5, and 6.

Claims 7 and 10-13

Independent claim 7, as amended, includes a limitation that is very similar in character to the limitation of claim 1 discussed above relative to the circuit that compensates for any delay in the first clock signal. In the case of independent claim 7, this claim requires a "circuit element adapted for generating a second clock signal that compensates for any delay in said first clock signal." In the same manner that Gregor et al. fail to disclose or suggest a circuit having this compensation feature, Gregor et al. also fail to disclose or suggest a circuit element having this feature. Therefore, the Gregor et al. patent cannot anticipate claim 7, nor claims 10-13 that depend therefrom.

In addition, claim 12 requires, by its dependency from claims 7 and 11, that the integrated circuit include a plurality of shift-register latches each having the unique timing-compensation circuit element of claim 7, as well as a plurality of shift-register latches that do not have these timing-compensation circuit elements. Gregor et al. are silent on having two sets of shift-register

latches differing by the presence/absence of a timing-compensation circuit element. For this additional reason, the Gregor et al. patent cannot anticipate claim 12.

For at least the foregoing reasons, Applicants respectfully request that the Examiner withdraw the present rejection of claims 7 and 10-13.

Rejection Under 35 U.S.C. § 103(a)

Claims 4, 8, and 9-20 stand rejected under 35 U.S.C. § 103(a) as obvious in view of a combination of U.S. Patent Application No. 2004/0061539 to Joordens et al. and the Gregor et al. patent, discussed above.

The Joordens et al. patent discloses a clock recovery circuit to correct the timing relationship between a data signal and a clock signal. This circuit includes a phase detector that is "applicable to data and clock recovery at higher frequencies." Par. 007. This phase detector receives three input signals, e.g., "an input for receiving a clock signal, an input for receiving a data signal and an input for receiving a window signal." Abstract. The detector generates two outputs, an up and down pulse, through the application of at least two separate AND gates, as illustrated in FIGS. 1, 3A, 4A, 7 and 8.

Claim 4, 8, and 9

The Office Action states that Gregor et al. disclose all the limitations of claims 4, 8, and 9 except "an AND gate and an inverter." The Office Action further states that Joordens et al. disclose these missing limitations and asserts that it would have been obvious to a person having ordinary skill in the art at the time of the invention to add this limitation to the Gregor et al. device. Applicants respectfully disagree.

First, neither Gregor et al. nor Joordens et al. disclose or suggest a pulse generator that generates and provides a clock pulse to a first latch of a shift-register latch as required in claims 4, 8, and 9. For the Gregor et al. patent, the lack of such pulse generator is discussed in the context of claim 3. Joorden et al. are likewise silent on such a pulse generator, since there is no shift-register latch involved in their patent. Second, even though Joordens et al. show AND gates, none of these gates is used for the purposes recited in claims 4, 8 and 9. Third, there simply is no motivation to combine these references. The Office Action's general statement that "one of ordinary skill in the art would have found it obvious to use the phase detector of Joordens et al. to acquire distorted signals at very high data rates and to provide clock signal and retimed or recovered data as outputs" does not constitute a *prima facie* showing of obviousness.

The Office Action does not set forth any assertion specific to shift-register latches to which the present invention is directed. Applicants respectfully assert that the U.S. Patent and Trademark Office must make a more problem-specific argument to satisfy the *prima facie* case requirement of MPEP § 2143.

For at least the foregoing reasons, Applicants respectfully request that the Examiner withdraw the present rejection.

Claims 14-20

Regarding claims 14 and 15, the Office Action states that Gregor et al. disclose the limitations of these claims except "a power supply connected to the integrated circuit." The Office Action then states that Joordens et al. disclose this missing limitation and asserts that it would have been obvious to a person having ordinary skill in the art at the time of the invention to add this limitation to the Jaeschke et al. apparatus. Applicants respectfully disagree.

Independent claim 14, like independent claim 1 discussed above, requires a "circuit, connected between said input and said first latch, configured for generating a second clock signal that compensates for any delay in said first clock signal." [Emphasis added.] As discussed above relative to claim 1, Gregor et al. simply do not disclose or suggest this limitation. Joordens et al. obviously do not disclose or suggest this limitation since the subject matter of their patent is vastly different. Since neither of the patents disclose or suggest this limitation, neither independent claim 14, nor claims 15-20 that depend therefrom, is obvious in view of the combination.

In addition, each of claims 16-18 includes a limitation that corresponds to a limitation in corresponding respective ones of claims 3-5. As discussed above, Gregor et al. do not disclose or suggest these limitations. Joordens et al. do not disclose these limitations, either. Therefore, claims 16-18 are not obvious in view of the combination of the Gregor et al. and Joordens et al. patents for this additional reason.

For at least the foregoing reasons, Applicants respectfully request that the Examiner withdraw the present rejection.

CONCLUSION

In view of the foregoing, Applicants submit that claims 1-20, as amended, are in condition for allowance. Therefore, prompt issuance of a Notice of Allowance is respectfully

solicited. If any issues remain, the Examiner is encouraged to call the undersigned attorney at the number listed below.

Respectfully submitted,

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